

CLAIMS

1. A semiconductor device including a plurality of non-volatile memory cells arrayed in rows and columns, the semiconductor device comprising:

- (a) a semiconductor substrate comprising a first region of a first conductivity type;
- (b) a plurality of parallel pairs of parallel implant region lines of a second conductivity type in the first region, wherein each of the columns of the non-volatile memory cells overlaps a respective one of the pairs of the implant regions lines, respective subportions of one of the implant region lines of the pair comprise respective source regions for the respective memory cells of the respective column, respective subportions of the other implant region line of the pair comprise respective drain regions for the respective memory cells of the column, and respective subportions of the first region between the respective source and drain regions of the respective memory cells comprises respective channel regions of the respective memory cells of the column;
- (c) one or more dielectric region lines in the first region and parallel to the implant region lines, wherein at least one of the dielectric region lines is between adjacent said pairs of the implant region lines;
- (d) a tunnel dielectric layer formed in a vicinity of the source region of each of the non-volatile memory cells, wherein the tunnel dielectric layer is in contact with the respective source region;
- (e) a plurality of regions of a first polysilicon layer, wherein each said non-volatile memory cell has one of the first polysilicon layer regions over the source region and over and in contact with the tunnel dielectric layer, the first polysilicon region being a floating gate that terminates over the channel region without extending to the drain region of the memory cell;
- (f) a plurality of lines of a second polysilicon layer each extending perpendicularly to the implant region lines, wherein each said second polysilicon layer line integrally overlies all of the memory cells of a row and the dielectric region line between adjacent memory cells of the row,

and a respective subportion of the second polysilicon layer line is a control gate of each said memory cell of the row; and

(g) at each of the non-volatile memory cells, a dielectric layer separating the second polysilicon layer line from the region of, first region surface over the channel region, and the drain region.

2. The semiconductor device of claim 1, wherein the first region is formed in a second region of the semiconductor substrate, the second region is of the second conductivity type, and the semiconductor substrate is of the first conductivity type.

3. The semiconductor device of claim 1, wherein the regions of the first polysilicon layer each have a rectangular shape.

4. The semiconductor device of claim 1, wherein the dielectric region lines comprise a field oxide.

5. The semiconductor device of claim 1, wherein the dielectric region lines each comprise an oxide layer formed in a trench in the first region.

6. The semiconductor device of claim 1, wherein the semiconductor substrate is of the first conductivity type, and the first region is deeply diffused in the semiconductor substrate.

7. The semiconductor device of claim 1, further comprising a plurality of main bitlines coupled to a bitline decoder, and a plurality of pass transistors, wherein each said implant region line that includes the drain regions is coupled at an end thereof to a respective one of said main bitlines through one of the pass transistors.

8. The semiconductor device of claim 1, further comprising a plurality of pass transistors, wherein each said implant region line that comprises the source regions is coupled at an end thereof to a reference voltage source through a respective one of the pass transistors.

9. The semiconductor device of claim 8, further comprising at least one sense amplifier coupled to the bitline decoder.

10. The semiconductor device of claim 1, further comprising a plurality of first and second pass transistors, wherein one of the first pass transistors is coupled to a respective one of the implant region lines of each pair of implant region lines, one of the second pass transistors is coupled to the other one of the implant region lines of the pair of implant region lines, the first pass transistors have a common control line for operating the first pass transistors, and the second pass transistors have a common control line for operating the second pass transistors.

10. A semiconductor device comprising:

a first region of a first conductivity type in a semiconductor substrate;

at least one pair of parallel implant region lines of a second conductivity type in said first region; and

for each pair of parallel implant region lines, a column of plural non-volatile memory cells overlapping the respective pair of implant region lines, wherein one of the implant region lines of the pair includes a respective source region for each of the memory cells of the column, and the other implant region line of the pair includes a respective drain region for each of the memory cells of the column, with a respective subportion of the first region between the source and drain region of each of the memory cells comprising a channel region for the respective memory cell.

11. The semiconductor device of claim 10, wherein each of the non-volatile memory cells comprises:

a tunnel dielectric layer in contact with one of the implant region lines of the pair of implant region lines;

an electrically isolated floating gate over and in contact with the tunnel dielectric layer and extending only part of a distance between the source and drain regions; and

a control gate over the floating gate and extending the entire distance between the source and drain regions; and

a dielectric layer between the control gate and a surface of the first region.

12. The semiconductor device of claim 11, wherein the tunnel dielectric layer is in contact with the implant region line that includes the source regions for the memory cells of the column.

13. The semiconductor device of claim 11, wherein there are a plurality of said pairs of parallel implant region lines in the first region, a plurality of the columns of the non-volatile memory cells, and a plurality of rows of the non-volatile memory cells across said columns, and further comprising:

a plurality of parallel dielectric isolation region lines parallel to the implant region lines, wherein one of the dielectric isolation region lines is between adjacent said columns of the memory cells; and

a plurality of parallel conductive wordlines extending perpendicularly across the implant region lines, wherein each said wordline integrally overlies the memory cells of one of the rows of the memory cells and the dielectric isolation region line between adjacent memory cells of the row, and a respective subportion of the wordline is the control gate for each of the respective memory cells of the row.

14. The semiconductor device of claim 13, further comprising a row decoder circuit coupled to each of the plurality of wordlines.

15. The semiconductor device of claim 13, further comprising a plurality of main bitlines, a plurality of first pass transistors, and a plurality of second pass transistors, and a main bitline decoder circuit coupled to the main bitlines,

wherein for each column of non-volatile memory cells, the implant region line including the drain regions is coupled to a respective one of the main bitlines of through one of the first pass transistors, and the implant region line including the source regions is coupled to a reference voltage source through one of the second pass transistors.

16. The semiconductor device of claim 10, wherein each of the non-volatile memory cells of the column comprises an electrically isolated floating gate and a control gate over the floating gate.

17. The semiconductor device of claim 16, wherein there are a plurality of the pairs of implant region lines and a plurality of the columns of non-volatile memory cells; and

further comprising a plurality of wordlines each extending transversely to the pairs of implant region lines, with each said wordline integrally overlying an entire row of the non-volatile memory cells,

wherein a respective subportion of the wordline is the control gate for each of the respective memory cells of the row.

18. The semiconductor device of claim 17, further comprising a plurality of main bit lines, wherein each of said implant region line comprising the drain regions of each said column includes is coupled to the one of the main bitlines through a pass transistor.

19. The semiconductor device of claim 18, wherein the implant region line comprising the drain regions of each respective said column includes only a single contact, and the associated implant region line comprising the source regions of the column includes only a single contact.

20. The semiconductor device of claim 17, wherein the implant region line comprising the drain regions of each respective said column includes only a single coupling to a main bit line, and the associated implant region line comprising the source regions of the column includes only a single coupling to a reference voltage source.

21. A semiconductor device comprising:

at least one block of non-volatile memory cells arrayed in rows and columns in a first region of a first conductivity type in a semiconductor substrate;

a plurality parallel pairs of parallel implant region lines of a second conductivity type in the first region, wherein each said column of the memory cells overlaps one pair of the implant

region lines, wherein one of the implant region lines comprises the source region for each of the memory cells of the column, and the other of the implant region lines comprises the drain region for each of the memory cells of the column;

a plurality of floating gates, wherein each of the memory cells includes a floating gate over the source region of the memory cell;

a tunnel dielectric layer between the floating gate of each memory cell and the underlying source region;

at least one dielectric isolation region, wherein one of the dielectric isolation regions is between adjacent columns of the memory cells;

a plurality of conductive wordlines traversing the implant region lines, wherein each said wordline integrally overlies the memory cells of one of the rows and the dielectric isolation region between adjacent memory cells of the row, wherein a respective subportion of the wordline is a control gate for each respective memory cell of the row;

dielectric material separating the wordline from a surface of the first region and from the floating gate at each of the memory cells.

22. A method of making a nonvolatile memory including a plurality of non-volatile memory cells in rows and columns, the method comprising:

providing a first region of a first conductivity type in a semiconductor substrate;

forming a plurality of parallel pairs of implant regions in the first region in the form of parallel lines;

forming dielectric isolation region lines in the first region, said isolation region lines being parallel to the implant region lines, wherein one of the isolation region lines is between adjacent pairs of the implant region lines,

wherein respective subportions of one of the implant region lines of each pair will be a source region for each of a plurality of memory cells in a column of the memory cells, an adjacent respective subportion of the other of the implant region lines of the pair will be a drain region for each of the memory cells of the column, and a respective intervening portion of the first region between the diffusion region lines of the pair will be a channel region of the respective memory cell;

forming a plurality of tunnel dielectric layers on a top surface of the first region, with each of the memory cells including one of the tunnel dielectric layers in contact with the source of the memory cell;

depositing and patterning a first polysilicon layer to obtain polysilicon stripes, wherein the tunnel oxide layer at each of the memory cells is in contact with one of the first polysilicon layer stripes;

forming a first dielectric layer over a top surface of each of the first polysilicon layer stripes;

depositing a second polysilicon layer over the first dielectric layer, and patterning the second polysilicon layer to obtain stripes perpendicular to the pairs of implant region lines, with each said second polysilicon layer stripe overlying a plurality of memory cells of a row of the memory cells, the second polysilicon layer stripe being entirely separated from a surface of the first region by a dielectric layer; and

etching the first polysilicon layer using the second polysilicon layer stripes as a mask, in order to produce a rectangle of the first polysilicon layer at each of the memory cells.

23. The method of claim 22, wherein the first region is diffused in a second region of the second conductivity type that is more deeply diffused into the semiconductor substrate, and the semiconductor substrate is of the first conductivity type.

24. The method of claim 22, wherein first region is diffused into the semiconductor substrate, the semiconductor substrate also being of the first conductivity type.

25. The method of claim 22, wherein the first and second polysilicon layers are etched in a single etch step.

26. The method of claim 22, further comprising forming a plurality of dielectric isolation region lines in the first region, wherein one said dielectric isolation region is between adjacent columns of the memory cells and extends parallel to the implant region lines.

27. The method of claim 26, wherein forming a plurality of dielectric isolation region lines comprises forming a plurality of parallel trenches in the surface of the first region, and filling the trenches with a dielectric material.

28. The method of claim 27, wherein forming a plurality of implant region lines in the first region comprises implanting ions of the second conductivity type into the first region through sidewalls of the trenches prior to filling the trenches with the dielectric material.

29. The method of claim 22, wherein forming a plurality of dielectric isolation region lines comprises forming a plurality of parallel field oxide lines, with each of the field oxide lines being formed between adjacent pairs of the implant region lines.

30. A method for operating a non-volatile memory, the method comprising:

providing a non-volatile memory comprising rows and columns of non-volatile memory cells formed in a first region of a first conductivity type in a semiconductor substrate, wherein each of the memory cells has a floating gate overlaid by a control gate, each column of the memory cells overlaps one pair of a plurality of parallel pairs of parallel implant region lines of a second conductivity type formed in the first region, with one of the implant region lines forming respective drain regions for the memory cells of the column, the other implant region line of the respective pair forming respective source regions for the memory cells of the column, and a plurality of wordlines each integrally overlying one of the rows of memory cells, with the control gates of each of the memory cells of the respective row being a respective subportion of the overlying wordline;

reading from a selected memory cell by applying appropriate low positive voltages on the wordline overlying the selected memory cell and on the implant region line forming the drain for the selected memory cell, while the implant region line that includes the source region for the selected memory cell is grounded; and

writing to a selected memory cell by applying an appropriate high positive voltage on the wordline overlying the selected memory cell and grounding the implant region line that includes the drain region for the selected memory cell, while the implant region line forming the drain regions for each deselected said column of the memory cells and the wordline for each deselected said row of the memory cells are biased at low voltage levels.

31. The method of claim 30, wherein the first conductivity type is P-type, the first region is deeply diffused in the semiconductor substrate, and the semiconductor substrate is P-type, and further comprising: and further comprising:

erasing a selected row of the memory cells by applying a negative high voltage level on the overlying wordline, while grounding the wordline overlying each deselected said row of memory cells..

32. The method of claim 30, wherein the first conductivity type is P-type, the first region is formed in a second region that is deeply diffused in the semiconductor substrate, the second region is of the N-type, and the semiconductor substrate is P-type, and further comprising:

erasing a selected row of the memory cells by grounding the wordline overlying the selected row while applying a high positive voltage to the first region, the second region, and to the wordline overlying each deselected said row.

33. The method of claim 30, wherein during said writing, each deselected said wordline is coupled to a positive voltage that is less than approximately half of the voltage applied to the selected wordline.

34. A method of forming a transistor comprising:

forming two parallel trenches in a first region of a semiconductor substrate, said first region having a first conductivity type, wherein each trench has a sidewall that faces the sidewall of the other trench, with a portion of the first region between the facing sidewalls;

implanting ions of a second conductivity type in the facing sidewalls of the first and second trenches, whereby a source region of the transistor is formed in the sidewall of one said trench, a drain region of the transistor is formed in the sidewall of the other said trench, a channel region of the transistor is in the first region between the source and drain regions.

35. The method of claim 34, further comprising filling the two trenches with a dielectric material after said implanting

36. The method of claim 35, further comprising forming a conductive gate of the transistor over the channel region.

37. The method of claim 34, further comprising forming a conductive gate of the transistor over the channel region.

38. An integrated circuit comprising:

a semiconductor substrate including a first region of a first conductivity type;

parallel first and second trenches in the first region, the first and second trenches each having a sidewall, with the sidewall of the first trench facing the sidewall of the second trench;

a transistor comprising a source region of a second conductivity type implanted in the sidewall of the first trench, and a drain region of the second conductivity type implanted in the facing sidewall of the second trench, wherein a portion of the first region between source and the drain regions comprises a channel region of the transistor;

a gate over the channel region; and

a dielectric material filling the first and the second trenches.

39. The integrated circuit of claim 38, further comprising a plurality of the transistors, wherein the source regions of the transistors are part of a continuous line of a dopant of the second conductivity type in the sidewall of the first trench, and the drain regions of the plural transistors are part of a continuous line of the dopant in the sidewall of the second trench.

40. The integrated circuit of claim 39, wherein each said transistor comprises a nonvolatile memory cell.

41. The integrated circuit of claim 38, wherein a plurality of the transistors are formed between the facing sidewalls first and second trenches.

42. The integrated circuit of claim 41, wherein the source regions of the plurality of transistors are respective subportions of a single implant region, and the drain regions of the plurality of transistors are respective subportions of a single implant region.

43. The integrated circuit of claim 39, wherein the gate comprises a floating gate overlaid by a control gate, wherein in the control gate is a subportion of a wordline that extends over dielectric material in the trench.

44. An integrated circuit comprising:

a semiconductor substrate including a first region of a first conductivity type;

a pair of parallel implant region lines of a second conductivity type in the first region;

a pair of field oxide region lines parallel to the implant region lines, wherein a bird's beak region of one of the field oxide region lines of the pair faces a bird's beak region of the other field oxide region line of the pair, with the pair of implant region lines being within the pair of field oxide region lines; and

a plurality of transistors formed between the pair of field oxide region lines, wherein each said transistor includes a source region that is a subportion of one of the implant region lines and a drain region that is a subportion of the other implant region line, and a gate overlying a surface of the first region.

45. The integrated circuit of claim 44, wherein the gate comprises a floating gate and a control gate.

46. The integrated circuit of claim 45, wherein the control gate is a subportion of a wordline that extends over the pair of field oxide region lines.

47. A non-volatile memory, comprising:

a plurality of non-volatile memory cells in a row in a first region of a semiconductor substrate, wherein each said memory cell has a source region, a drain region, a channel region between the source and drain regions, and a floating gate;

one or more dielectric isolation regions, wherein one of the isolation regions is between adjacent memory cells of the row;

a polysilicon layer extending integrally over the plurality of the memory cells of the row and over each said intervening dielectric isolation region, wherein an integral subportion of the polysilicon layer over each of the respective memory cells forms a control gate for the memory cell.

48. The non-volatile memory of claim 47, further comprising a plurality of the rows of the memory cells, arranged so the memory cells of the plurality of rows form columns of the memory cells, with each row having a separate overlying one of the polysilicon layers.

49. The non-volatile memory of claim 48, wherein the source regions of each memory cell of each said column of the memory cells are respective subportions of a contiguous first implant region line in the first region, the drain regions of each memory cell of each said column are respective subportions of a contiguous second implant region line in the first region, said second implant region line being parallel to the first implant region line.

50. An integrated circuit comprising:

a first region of a first conductivity type in a semiconductor substrate;

parallel first and second implant region lines of a second conductivity type in the first region;

a plurality of conductive first gates overlying a surface of the first region between the first and second implant region lines, wherein each said first gate is part of one of a plurality of transistors overlapping the first and second implant region lines, with each said transistor including a subportion of the first implant line as a source region, a subportion of the second implant line as a drain region, and a subportion of the first region between the source and drain regions as a channel region.

51. The integrated circuit of claim 50, wherein each said transistor is a non-volatile memory cell.

52. The integrated circuit of claim 50, wherein the first gate is a floating gate, and further comprising a control gate over the first gate.